

10-Bit, 105Msps, Single +3.3V, Low-Power ADC with Internal Reference

General Description

The MAX1449 +3.3V, 10-bit analog-to-digital converter (ADC) features a fully differential input, a pipelined 10-stage ADC architecture with wideband track-and-hold (T/H), and digital error correction incorporating a fully differential signal path. The ADC is optimized for low-power, high-dynamic performance in imaging and digital communications applications. The converter operates from a single +2.7V to +3.6V supply, consuming only 186mW while delivering a 58.5dB (typ) signal-to-noise ratio (SNR) at a 20MHz input frequency. The fully differential input stage has a -3dB 400MHz bandwidth and may be operated with single-ended inputs. In addition to low operating power, the MAX1449 features a 5 μ A power-down mode for idle periods.

An internal +2.048V precision bandgap reference is used to set the ADC's full-scale range. A flexible reference structure allows the user to supply a buffered, direct, or externally derived reference for applications requiring increased accuracy or a different input voltage range.

Lower speed, pin-compatible versions of the MAX1449 are also available. Refer to the MAX1444 data sheet for a 40Msps version, the MAX1446 data sheet for a 60Msps version, and the MAX1448 data sheet for 80Msps.

The MAX1449 has parallel, offset binary, CMOS-compatible, three-state outputs that can be operated from +1.7V to +3.6V to allow flexible interfacing. The device is available in a 5mm x 5mm 32-pin TQFP package and is specified over the extended industrial (-40°C to +85°C) temperature range.

Applications

- Ultrasound Imaging
- CCD Imaging
- Baseband and IF Digitization
- Digital Set-Top Boxes
- Video Digitizing Applications

Pin Configuration appears at end of data sheet.

Features

- ◆ Single +3.3V Operation
- ◆ Excellent Dynamic Performance
 - 58.5dB SNR at $f_{IN} = 20\text{MHz}$
 - 72dBc SFDR at $f_{IN} = 20\text{MHz}$
- ◆ Low Power
 - 62mA (Normal Operation)
 - 5 μ A (Shutdown Mode)
- ◆ Fully Differential Analog Input
- ◆ Wide 2Vp-p Differential Input Voltage Range
- ◆ 400MHz -3dB Input Bandwidth
- ◆ On-Chip +2.048V Precision Bandgap Reference
- ◆ CMOS-Compatible Three-State Outputs
- ◆ 32-Pin TQFP Package
- ◆ Evaluation Kit Available

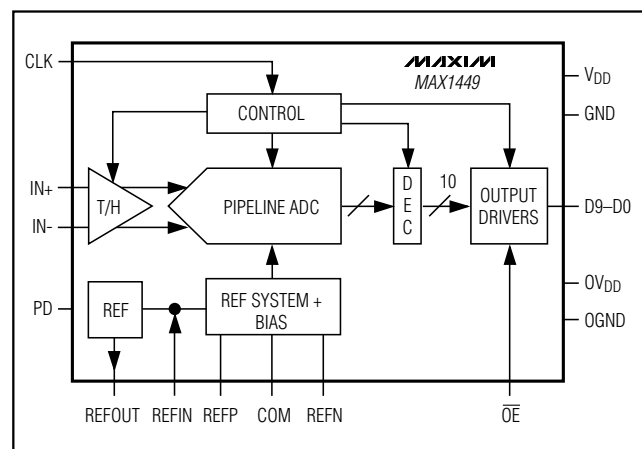
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1449EHJ	-40°C to +85°C	32 TQFP

Pin-Compatible, Lower Speed Selection Table

PART NUMBER	SAMPLING SPEED
MAX1444	40Msps
MAX1446	60Msps
MAX1448	80Msps

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

V _{DD} , OV _{DD} to GND	-0.3V to +3.6V	Continuous Power Dissipation (T _A = +70°C)	
OGND to GND	-0.3V to +0.3V	32-Pin TQFP (derate 11.1mW/°C above +70°C)	889mW
IN+, IN- to GND	-0.3V to V _{DD}	Operating Temperature Range	-40°C to +85°C
REFIN, REFOUT, REFP,		Junction Temperature	+150°C
REFN, and COM to GND	-0.3V to (V _{DD} + 0.3V)	Storage Temperature Range	-60°C to +150°C
OE, PD, CLK to GND	-0.3V to (V _{DD} + 0.3V)	Lead Temperature (soldering, 10s)	+300°C
D9–D0 to GND	-0.3V to (OV _{DD} + 0.3V)		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3.3V, OV_{DD} = +2.0V; 0.1μF and 1.0μF capacitors from REFP, REFN, and COM to GND; V_{REFIN} = +2.048V, REFOUT connected to REFIN through a 10kΩ resistor, V_{IN} = 2Vp-p (differential with respect to COM), C_L ≈ 10pF at digital outputs, f_{CLK} = 105MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			10			Bits
Integral Nonlinearity	INL	f _{IN} = 7.5MHz		±0.75	±2.4	LSB
Differential Nonlinearity	DNL	f _{IN} = 7.5MHz, no missing codes guaranteed		±0.5	±1.0	LSB
Offset Error				< ±1	±1.7	% FS
Gain Error				0	±2	% FS
ANALOG INPUT						
Input Differential Range	V _{DIFF}	Differential or single-ended inputs		±1.0		V
Common-Mode Voltage Range	V _{COM}			V _{DD} /2 ±0.5		V
Input Resistance	R _{IN}	Switched capacitor load		20		kΩ
Input Capacitance	C _{IN}			5		pF
CONVERSION RATE						
Maximum Clock Frequency	f _{CLK}		105			MHz
Data Latency				5.5		Cycles
DYNAMIC CHARACTERISTICS (f _{CLK} = 105.26MHz, 4096-point FFT)						
Signal-To-Noise Ratio (Note 1)	SNR	f _{IN} = 7.5MHz	56.3	58.5		dB
		f _{IN} = 20MHz	55.8	58.5		
		f _{IN} = 50MHz		58		
Signal-To-Noise And Distortion (Up to 5 th Harmonic) (Note 1)	SINAD	f _{IN} = 7.5MHz	55.3	58.2		dB
		f _{IN} = 20MHz	55.1	58.1		
		f _{IN} = 50MHz		57.6		
Spurious-Free Dynamic Range (Note 1)	SFDR	f _{IN} = 7.5MHz	61	72		dBc
		f _{IN} = 20MHz, T _A = +25°C	63	72		
		f _{IN} = 50MHz		70		

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +3.3V$, $OV_{DD} = +2.0V$; 0.1 μF and 1.0 μF capacitors from REFP, REFN, and COM to GND; $V_{REFIN} = +2.048V$, REFOUT connected to REFIN through a 10k Ω resistor, $V_{IN} = 2V_{p-p}$ (differential with respect to COM), $C_L \approx 10pF$ at digital outputs, $f_{CLK} = 105MHz$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Third-Harmonic Distortion (Note 1)	HD3	$f_{IN} = 7.5MHz$		-72		dBc
		$f_{IN} = 20MHz$		-72		
		$f_{IN} = 50MHz$		-70		
Intermodulation Distortion (First 5 Odd-Order IMDs) (Note 2)	IMD	$f_1 = 38MHz$ at -6.5dB FS $f_2 = 42MHz$ at -6.5dB FS		-76		dBc
Third-Order Intermodulation Distortion (Note 2)	IM3	$f_1 = 38MHz$ at -6.5dB FS $f_2 = 42MHz$ at -6.5dB FS		-76		dBc
Total Harmonic Distortion (First 5 Harmonics) (Note 1)	THD	$f_{IN} = 7.5MHz$, $T_A = +25^\circ C$		-70	-61.5	dBc
		$f_{IN} = 20MHz$, $T_A = +25^\circ C$		-70	-61.5	
		$f_{IN} = 50MHz$		-70		
Small-Signal Bandwidth		Input at -20dB FS, differential inputs		500		MHz
Full-Power Bandwidth	FPBW	Input at -0.5dB FS, differential inputs		400		MHz
Aperture Delay	t_{AD}			1		ns
Aperture Jitter	t_{AJ}			2		psRMS
Overdrive Recovery Time		For 1.5 x full-scale input		2		ns
Differential Gain				± 1		%
Differential Phase				± 0.25		degree
Output Noise		IN+ = IN- = COM		0.2		LSBRMS
INTERNAL REFERENCE						
Reference Output Voltage	REFOUT			2.048 $\pm 1\%$		V
Reference Temperature Coefficient	TC_{REF}			60		ppm/ $^\circ C$
Load Regulation				1.25		mV/mA
EXTERNAL REFERENCE						
Positive Reference	REFP	$V_{REFIN} = +2.048V$		2.162		V
Negative Reference	REFN	$V_{REFIN} = +2.048V$		1.138		V
Differential Reference Voltage	ΔV_{REF}	$V_{REFP} - V_{REFN}$, $V_{REFIN} = +2.048V$	0.98	1.024	1.07	V
REFIN Resistance	R_{REFIN}			>50		M Ω
DIGITAL INPUTS (CLK, PD, \overline{OE})						
Input High Threshold	V_{IH}	CLK		0.8 x V_{DD}		V
		PD, \overline{OE}		0.8 x V_{DD}		
Input Low Threshold	V_{IL}	CLK			0.2 x V_{DD}	V
		PD, \overline{OE}			0.2 x V_{DD}	

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ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Hysteresis	V_{HYST}			0.1		V
Input Leakage	I_{IH}	$V_{IH} = V_{DD} = OV_{DD}$			± 5	μA
	I_{IL}	$V_{IL} = 0$			± 5	
Input Capacitance	C_{IN}			5		pF
DIGITAL OUTPUTS (D9–D0)						
Output Voltage Low	V_{OL}	$I_{SINK} = 200\mu A$			0.2	V
Output Voltage High	V_{OH}	$I_{SOURCE} = 200\mu A$	OV_{DD} -0.2			V
Three-State Leakage Current	I_{LEAK}	$\overline{OE} = OV_{DD}$			± 10	μA
Three-State Output Capacitance	C_{OUT}	$\overline{OE} = OV_{DD}$		5		pF
POWER REQUIREMENTS						
Analog Supply Voltage	V_{DD}		2.7	3.3	3.6	V
Output Supply Voltage	OV_{DD}		1.7	3.3	3.6	V
Analog Supply Current	I_{VDD}	Operating, $f_{IN} = 20MHz$ at -0.5dB FS		58	74	mA
		Shutdown, clock idle, $PD = \overline{OE} = OV_{DD}$		4	15	μA
Output Supply Current	I_{OVDD}	Operating, $C_L = 15pF$, $f_{IN} = 20MHz$ at -0.5dB FS		10		mA
		Shutdown, clock idle, $PD = \overline{OE} = OV_{DD}$		1	10	μA
Power Supply Rejection	PSRR	Offset		± 0.1		mV/V
		Gain		± 0.1		%/V
TIMING CHARACTERISTICS						
CLK Rise-to-Output Data Valid	t_{DO}	Figure 6 (Note 3)		5	8	ns
\overline{OE} Fall-to-Output Enable	t_{ENABLE}	Figure 5		10		ns
\overline{OE} Rise-to-Output Disable	$t_{DISABLE}$	Figure 5		15		ns
CLK Pulse Width High	t_{CH}	Figure 6, clock period 9.52ns		4.76 ± 0.47		ns
CLK Pulse Width Low	t_{CL}	Figure 6, clock period 9.52ns		4.76 ± 0.47		ns
Wake-Up Time	t_{WAKE}	(Note 4)		1.5		μs

Note 1: SNR, SINAD, THD, SFDR and HD3 are based on an analog input voltage of -0.5dB FS referenced to a +1.024V full-scale input voltage range.

Note 2: Intermodulation distortion is the total power of the intermodulation products relative to the individual carrier. This number is 6dB better if referenced to the two-tone envelope.

Note 3: Digital outputs settle to V_{IH}, V_{IL} .

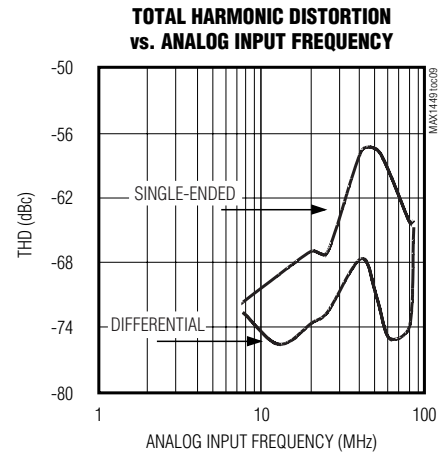
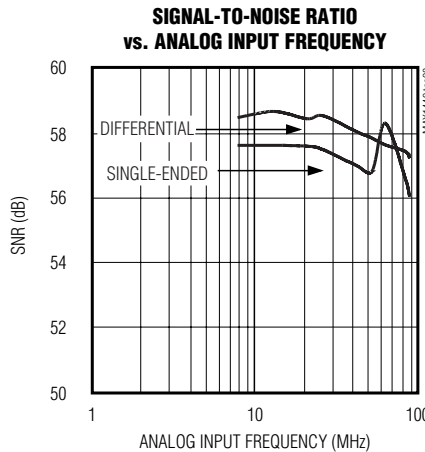
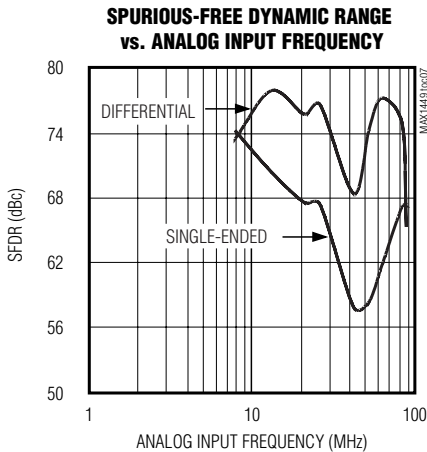
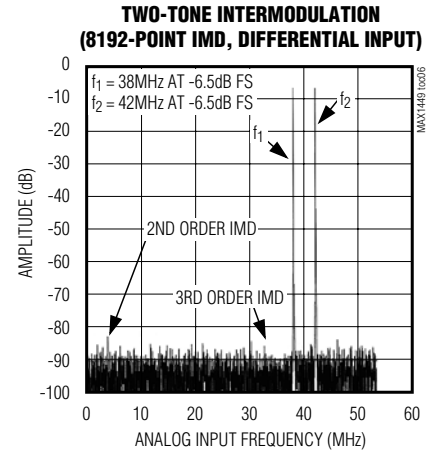
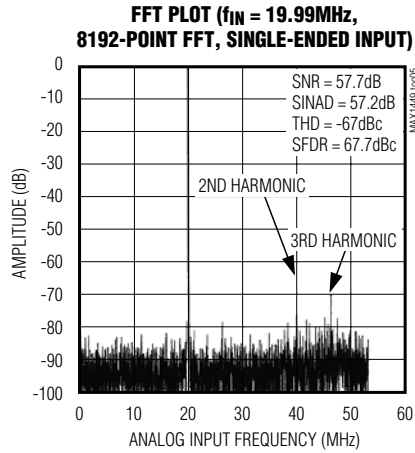
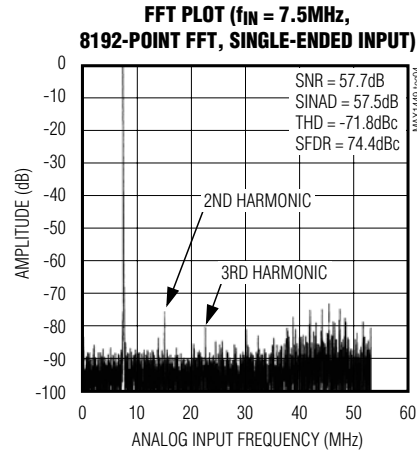
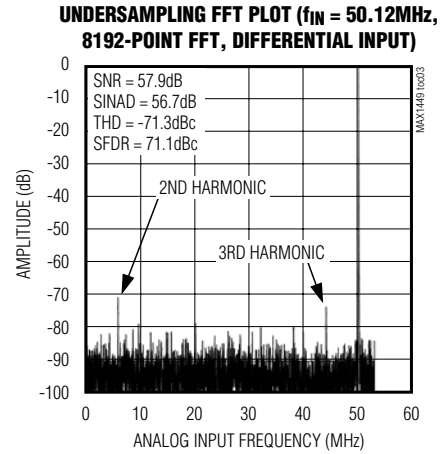
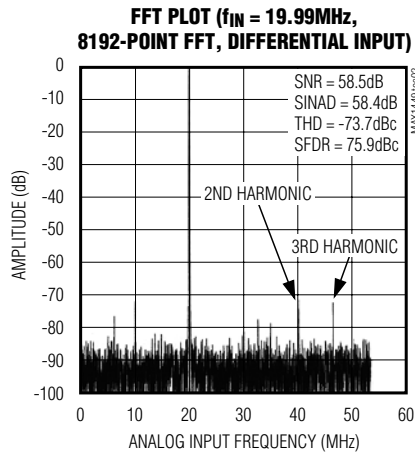
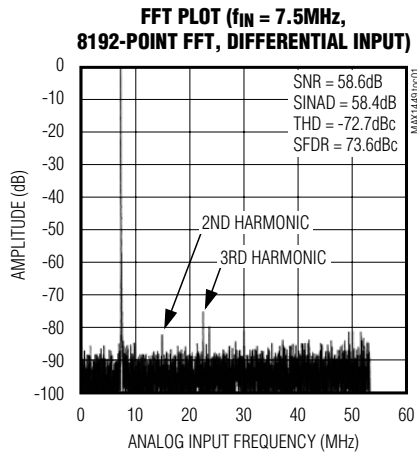
Note 4: With REFIN driven externally, REFP, COM, and REFN are left floating while powered down.

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Typical Operating Characteristics

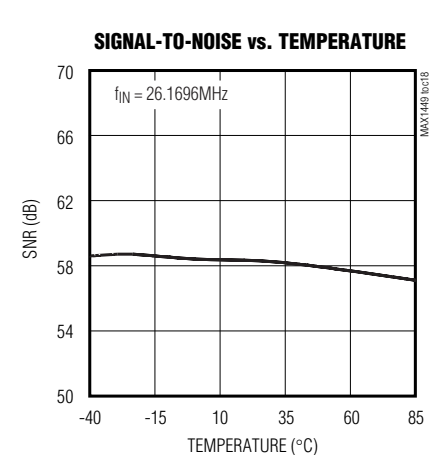
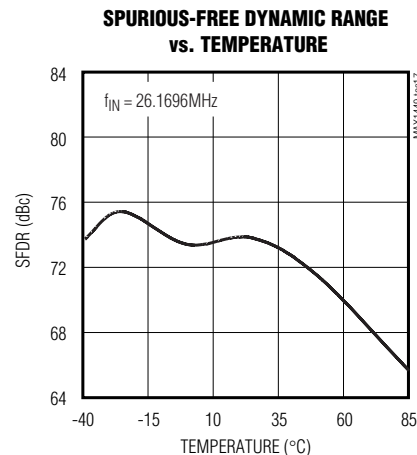
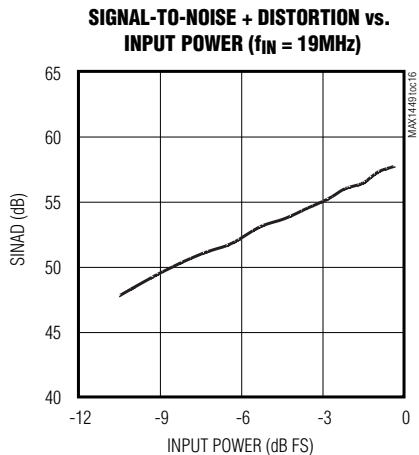
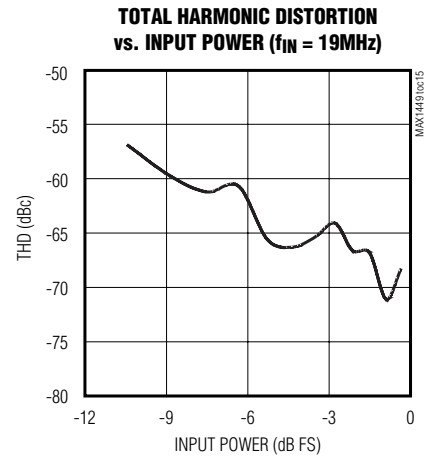
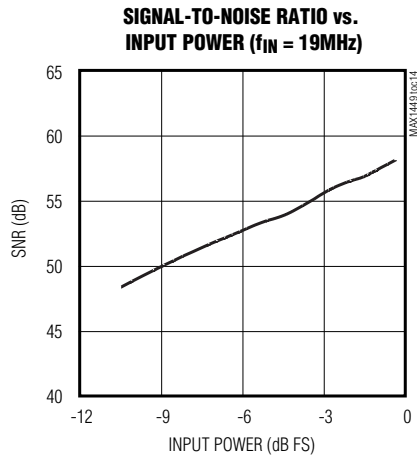
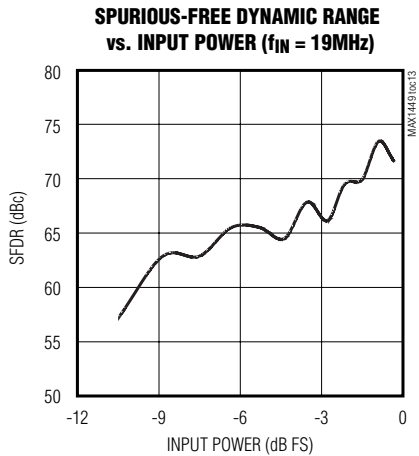
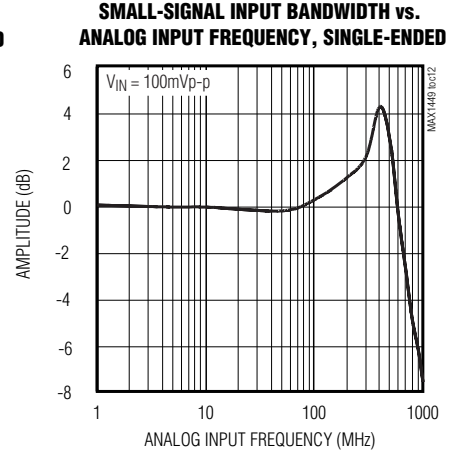
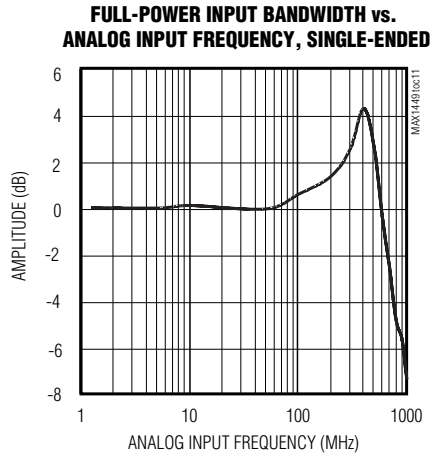
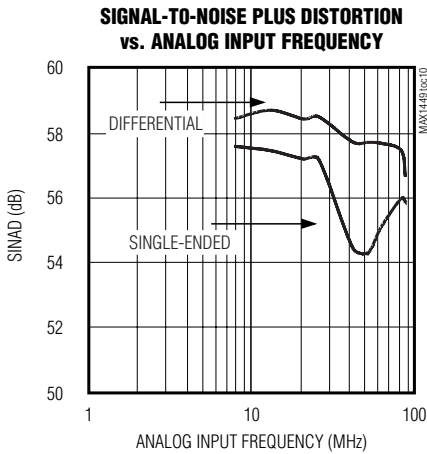
($V_{DD} = +3.3V$, $OV_{DD} = +2.0V$, internal reference, differential input at $-0.5dB$ FS, $f_{CLK} = 106.2345MHz$, $C_L \approx 10pF$, $T_A = +25^\circ C$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

($V_{DD} = +3.3V$, $OV_{DD} = +2.0V$, internal reference, differential input at $-0.5dB$ FS, $f_{CLK} = 106.2345MHz$, $C_L \approx 10pF$, $T_A = +25^\circ C$, unless otherwise noted.)

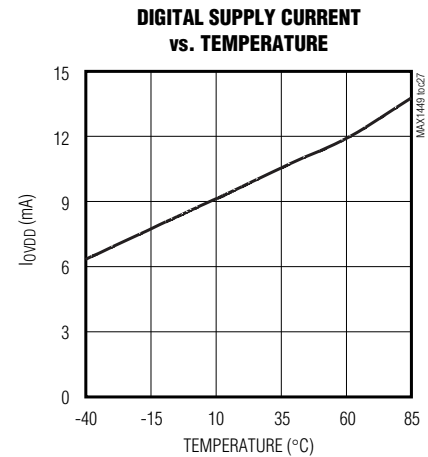
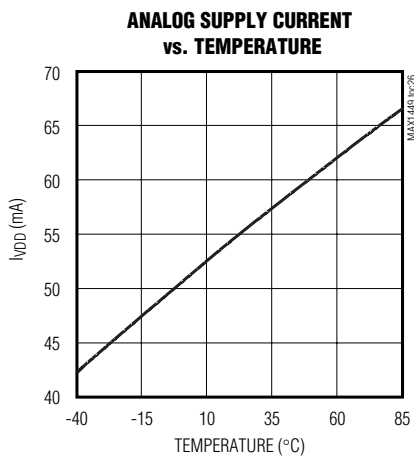
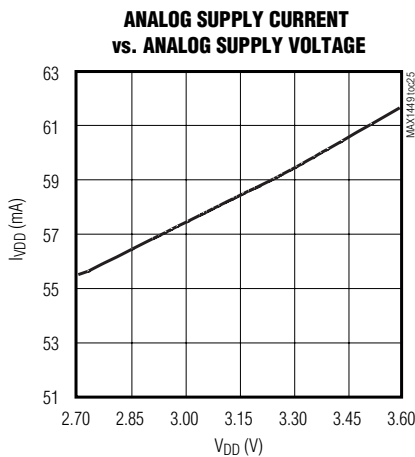
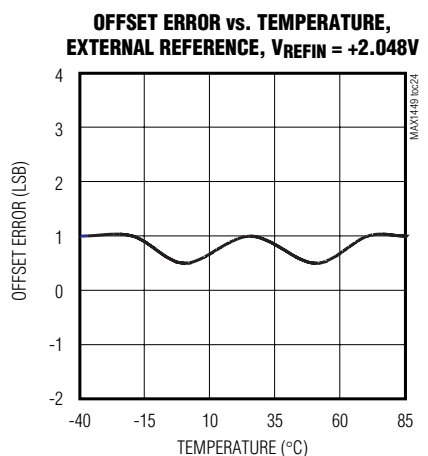
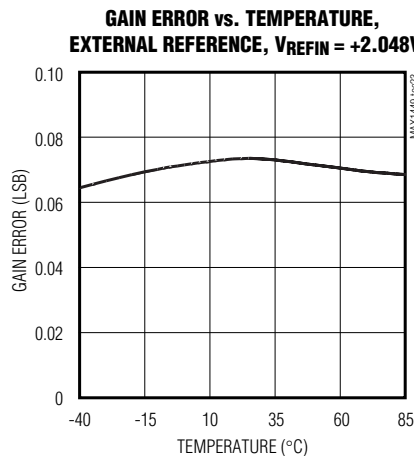
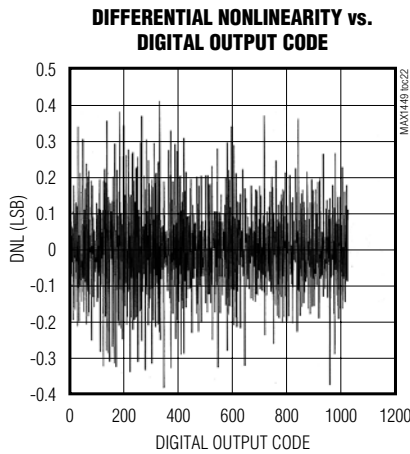
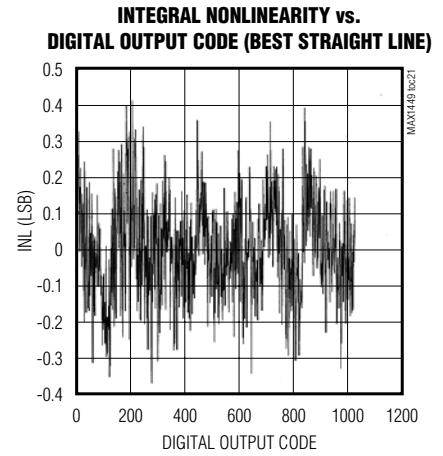
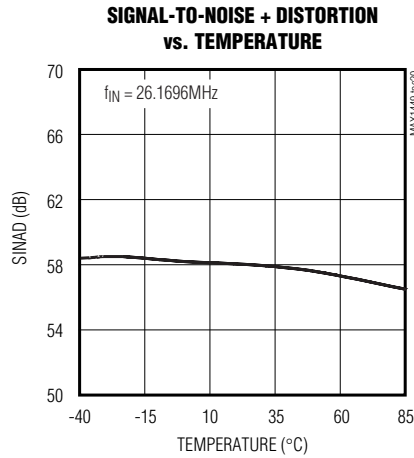
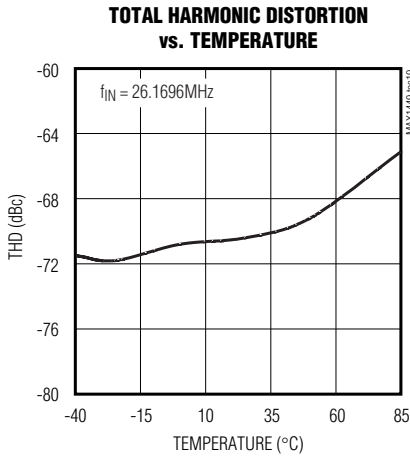


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Typical Operating Characteristics (continued)

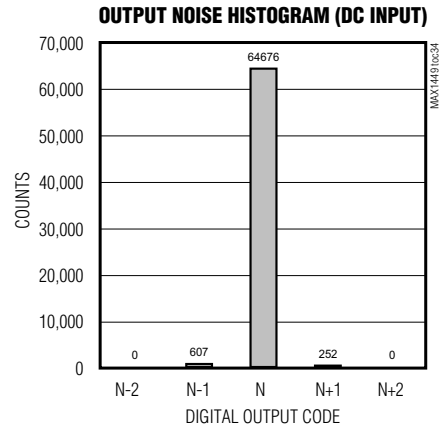
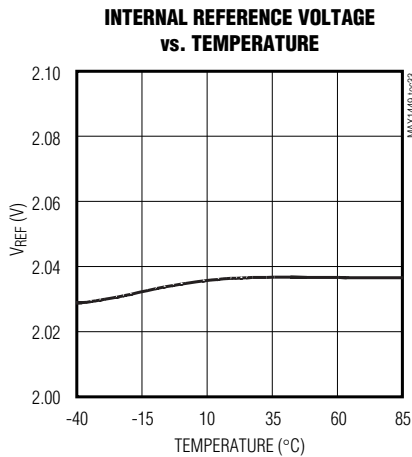
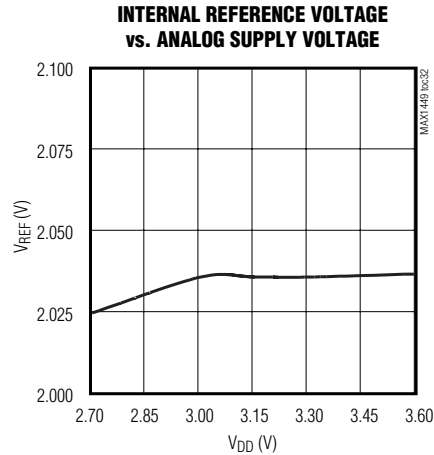
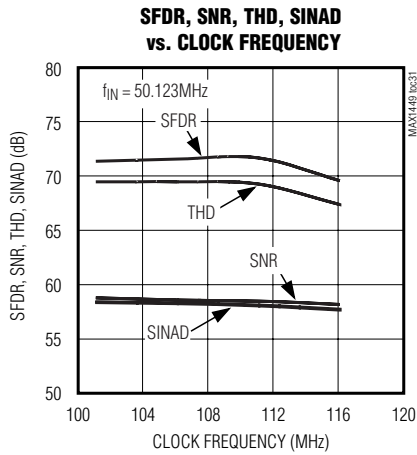
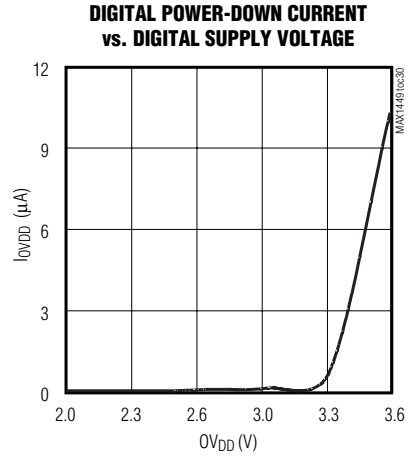
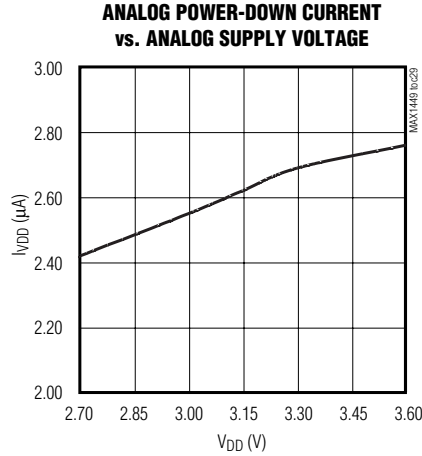
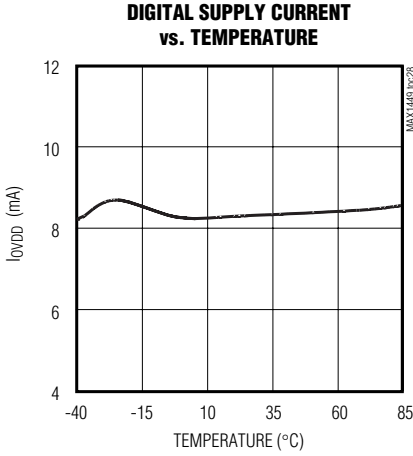
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Typical Operating Characteristics (continued)

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Pin Description

MAX1449

PIN	NAME	FUNCTION
1	REFN	Lower Reference. Conversion range is $\pm(V_{REFP} - V_{REFN})$. Bypass to GND with a $> 0.1\mu\text{F}$ capacitor.
2	COM	Common-Mode Voltage Output. Bypass to GND with a $> 0.1\mu\text{F}$ capacitor.
3, 9, 10	V _{DD}	Analog Supply Voltage. Bypass to GND with a capacitor combination of $2.2\mu\text{F}$ in parallel with $0.1\mu\text{F}$.
4, 5, 8, 11, 14, 30	GND	Analog Ground
6	IN+	Positive Analog Input. For single-ended operation connect signal source to IN+.
7	IN-	Negative Analog Input. For single-ended operation connect IN- to COM.
12	CLK	Conversion Clock Input
13	PD	Power Down Input. High: Power-down mode Low: Normal operation
15	$\overline{\text{OE}}$	Output Enable Input. High: Digital outputs disabled Low: Digital outputs enabled
16–20	D9–D5	Three-State Digital Outputs D9–D5. D9 is the MSB.
21	OV _{DD}	Output Driver Supply Voltage. Bypass to GND with a capacitor combination of $2.2\mu\text{F}$ in parallel with $0.1\mu\text{F}$.
22	T.P.	Test Point. Do not connect.
23	OGND	Output Driver Ground
24–28	D4–D0	Three-State Digital Outputs D4–D0. D0 is the LSB.
29	REFOUT	Internal Reference Voltage Output. May be connected to REF _{IN} through a resistor or a resistor-divider.
31	REF _{IN}	Reference Input. $V_{REFIN} = 2 \times (V_{REFP} - V_{REFN})$. Bypass to GND with a $> 0.1\mu\text{F}$ capacitor.
32	REFP	Upper Reference. Conversion range is $\pm(V_{REFP} - V_{REFN})$. Bypass to GND with a $> 0.1\mu\text{F}$ capacitor.

10-Bit, 105MSPS, Single +3.3V, Low-Power ADC with Internal Reference

Detailed Description

The MAX1449 uses a 10-stage, fully differential, pipelined architecture (Figure 1), that allows for high-speed conversion while minimizing power consumption. Each sample moves through a pipeline stage every half-clock cycle. Counting the delay through the output latch, the clock-cycle latency is 5.5.

A 1.5-bit (2-comparator) flash ADC converts the held input voltage into a digital code. The following digital-to-analog converter (DAC) converts the digitized result back into an analog voltage, which is then subtracted from the original held input signal. The resulting error signal is then multiplied by two, and the product is passed along to the next pipeline stage where the process is repeated until the signal has been processed by all 10 stages. Each stage provides a 1-bit resolution. Digital error-correction compensates for ADC comparator offsets in each pipeline stage and ensures no missing codes.

Input Track-and-Hold (T/H) Circuit

Figure 2 displays a simplified functional diagram of the input track-and-hold (T/H) circuit in both track and hold mode. In track mode, switches S1, S2a, S2b, S4a, S4b, S5a and S5b are closed. The fully differential circuit samples the input signal onto the two capacitors C2a and C2b through switches S4a and S4b. Switches S2a and S2b set the common mode for the amplifier input,

and open simultaneously with S1, sampling the input waveform. Switches S4a and S4b are then opened before switches S3a and S3b connect capacitors C1a and C1b to the output of the amplifier and switch S4c is closed. The resulting differential voltage is held on capacitors C2a and C2b. The amplifier is used to charge capacitors C1a and C1b to the same values originally held on C2a and C2b. This value is then presented to the first stage quantizer and isolates the pipeline from the fast-changing input. The wide input bandwidth T/H amplifier allows the MAX1449 to track and sample/hold analog inputs of high frequencies beyond Nyquist. The analog inputs IN+ and IN- can be driven either differentially or single-ended. It is recommended to match the impedance of IN+ and IN- and set the common-mode voltage to mid-supply ($V_{DD}/2$) for optimum performance.

Analog Input and Reference Configuration

The full-scale range of the MAX1449 is determined by the internally generated voltage difference between REFP ($V_{DD}/2 + V_{REFIN}/4$) and REFN ($V_{DD}/2 - V_{REFIN}/4$). The ADC's full-scale range is user-adjustable through the REFIN pin, which provides a high input impedance for this purpose. REFOUT, REFP, COM ($V_{DD}/2$), and REFN are internally buffered low-impedance outputs.

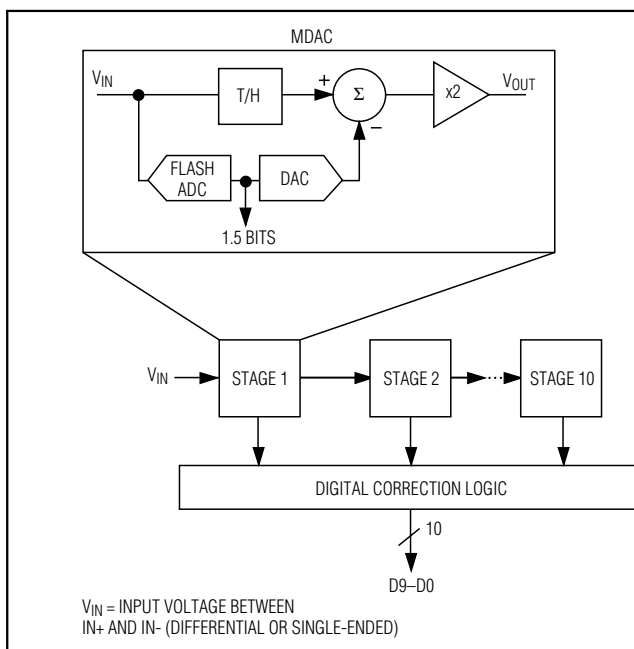


Figure 1. Pipelined Architecture—Stage Blocks

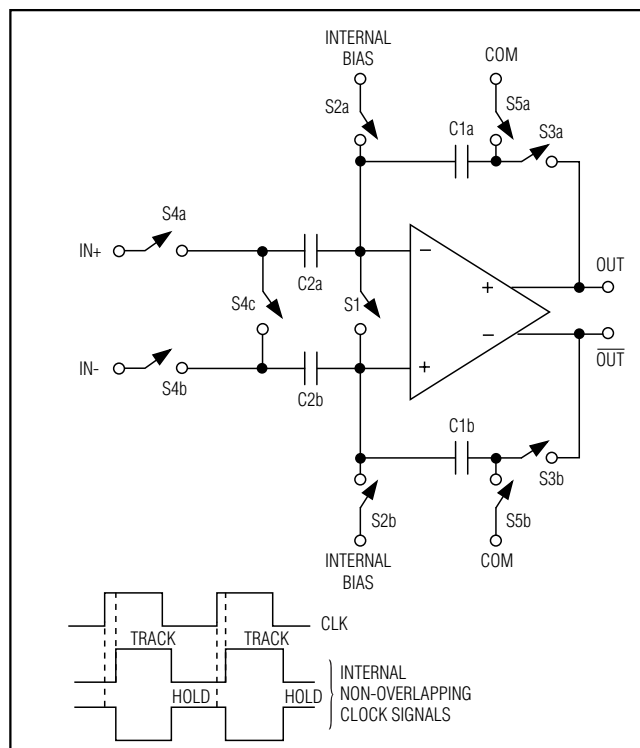


Figure 2. Internal T/H Circuit

10-Bit, 105MSPS, Single +3.3V, Low-Power ADC with Internal Reference

The MAX1449 provides three modes of reference operation:

- Internal reference mode
- Buffered external reference mode
- Unbuffered external reference mode

In internal reference mode, the internal reference output REFOUT can be tied to the REFIN pin through a resistor (e.g., 10k Ω) or resistor-divider, if an application requires a reduced full-scale range. For stability purposes it is recommended to bypass REFIN with a >10nF capacitor to GND.

In buffered external reference mode, the reference voltage levels can be adjusted externally by applying a stable and accurate voltage at REFIN. In this mode, REFOUT may be left open or connected to REFIN through a >10k Ω resistor.

In unbuffered external reference mode, REFIN is connected to GND thereby deactivating the on-chip buffers of REFP, COM, and REFN. With their buffers shut down, these pins become high impedance and can be driven by external reference sources.

Clock Input (CLK)

The MAX1449's CLK input accepts CMOS-compatible clock signals. Since the inter-stage conversion of the device depends on the repeatability of the rising and falling edges of the external clock, use a clock with low jitter and fast rise and fall times (<2ns). In particular, sampling occurs on the falling edge of the clock signal, mandating this edge to provide lowest possible jitter. Any significant aperture jitter would limit the SNR performance of the ADC as follows:

$$\text{SNR} = 20 \times \log(0.5 \times \pi \times f_{\text{IN}} \times t_{\text{AJ}})$$

where f_{IN} represents the analog input frequency and t_{AJ} is the time of the aperture jitter.

Clock jitter is especially critical for undersampling applications. The clock input should always be consid-

ered as an analog input and routed away from any analog input or other digital signal lines.

The MAX1449 clock input operates with a voltage threshold set to $V_{\text{DD}}/2$. Clock inputs with a duty cycle other than 50% must meet the specifications for high and low periods as stated in the *Electrical Characteristics*. (See Figures 3 (3a, 3b) and 4 (4a, 4b) for the relationship between spurious-free dynamic range (SFDR), signal-to-noise ratio (SNR), total harmonic distortion (THD), or signal-to-noise plus distortion (SINAD) versus duty cycle.)

Output Enable ($\overline{\text{OE}}$), Power Down (PD), and Output Data (D0–D9)

All data outputs, D0 (LSB) through D9 (MSB), are TTL/CMOS logic-compatible. There is a 5.5 clock-cycle latency between any particular sample and its valid output data. The output coding is straight offset binary (Table 1). With $\overline{\text{OE}}$ and PD high, the digital outputs enter a high-impedance state. If $\overline{\text{OE}}$ is held low with PD high, the outputs are latched at the last value prior to the power down.

The capacitive load on the digital outputs D0 through D9 should be kept as low as possible (<15pF), to avoid large digital currents that could feed back into the analog portion of the MAX1449, thereby degrading its dynamic performance. The use of buffers on the digital outputs of the ADC can further isolate the digital outputs from heavy capacitive loads. To further improve the dynamic performance of the MAX1449, small series resistors (e.g., 100 Ω) may be added to the digital output paths, close to the ADC. Figure 5 displays the timing relationship between output enable and data output valid as well as power-down/wake-up and data output valid.

System Timing Requirements

Figure 6 depicts the relationship between the clock input, analog input, and data output. The MAX1449 samples at the falling edge of the input clock. Output

Table 1. MAX1449 Output Code for Differential Inputs

DIFFERENTIAL INPUT VOLTAGE*	DIFFERENTIAL INPUT	STRAIGHT OFFSET BINARY
$V_{\text{REF}} \times 511/512$	+Full Scale -1LSB	11 1111 1111
$V_{\text{REF}} \times 510/512$	+Full Scale -2LSB	11 1111 1110
$V_{\text{REF}} \times 1/512$	+1LSB	10 0000 0001
0	Bipolar Zero	10 0000 0000
$-V_{\text{REF}} \times 1/512$	-1LSB	01 1111 1111
$-V_{\text{REF}} \times 511/512$	Negative Full Scale + 1LSB	00 0000 0001
$-V_{\text{REF}} \times 512/512$	Negative Full Scale	00 0000 0000

* $V_{\text{REF}} = V_{\text{REFP}} = V_{\text{REFN}}$

10-Bit, 105MSPS, Single +3.3V, Low-Power ADC with Internal Reference

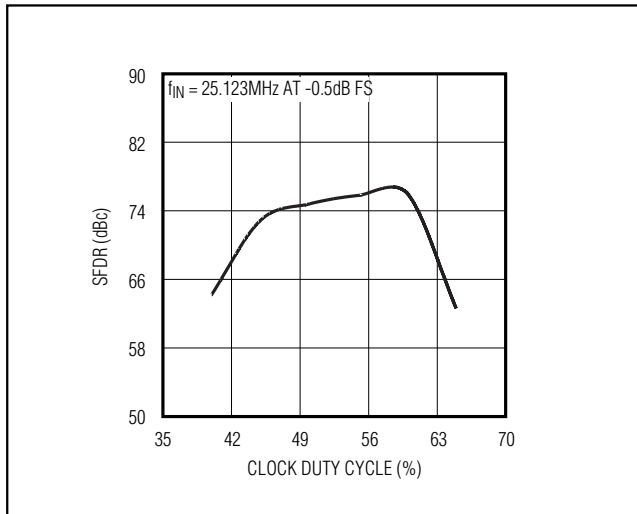


Figure 3a. Spurious Free Dynamic Range vs. Clock Duty Cycle (Differential Input)

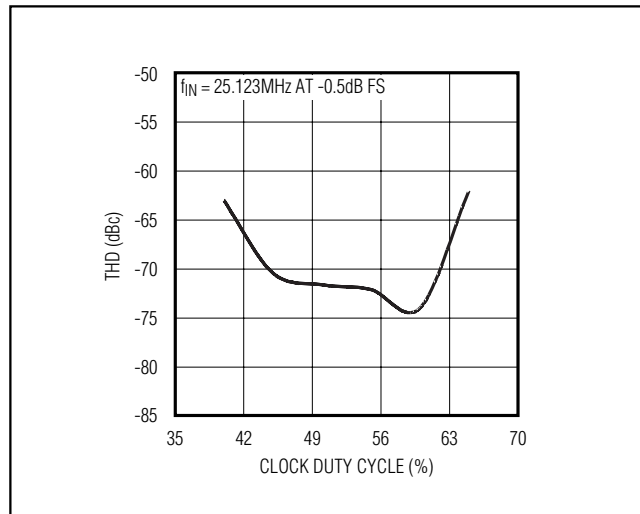


Figure 4a. Total Harmonic Distortion vs. Clock Duty Cycle (Differential Input)

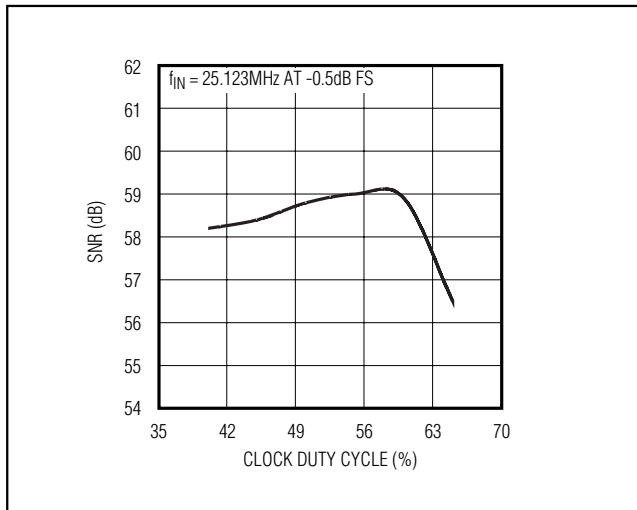


Figure 3b. Signal-to-Noise Ratio vs. Clock Duty Cycle (Differential Input)

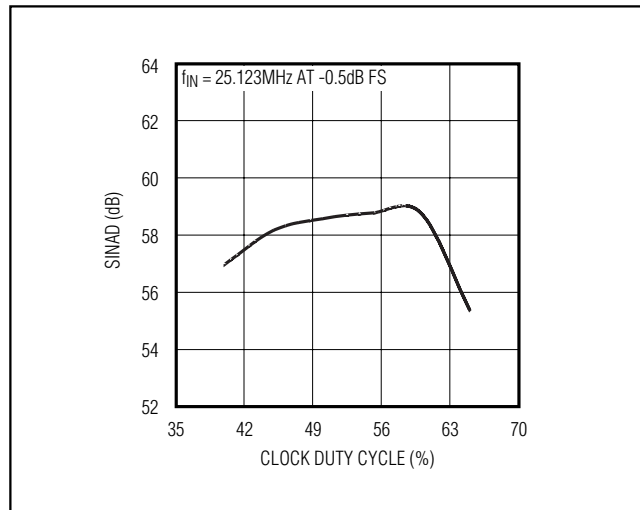


Figure 4b. Signal-to-Noise Plus Distortion vs. Clock Duty Cycle (Differential Input)

data is valid on the rising edge of the input clock. The output data has an internal latency of 5.5 clock cycles. Figure 6 also determines the relationship between the input clock parameters and the valid output data.

Applications Information

Figure 7 depicts a typical application circuit containing a single-ended to differential converter. The internal reference provides a $V_{DD}/2$ output voltage for level shifting purposes. The input is buffered and then split to a volt-

age follower and inverter. A low-pass filter, to suppress some of the wideband noise associated with high-speed op amps, follows the op amps. The user may select the R_{ISO} and C_{IN} values to optimize the filter performance, to suit a particular application. For the application in Figure 7, a R_{ISO} of 50Ω is placed before the capacitive load to prevent ringing and oscillation. The 22pF C_{IN} capacitor acts as a small bypassing capacitor.

10-Bit, 105Mps, Single +3.3V, Low-Power ADC with Internal Reference

Using Transformer Coupling

An RF transformer (Figure 8) provides an excellent solution to convert a single-ended source signal to a fully differential signal, required by the MAX1449 for optimum performance. Connecting the center tap of the transformer to COM provides a $V_{DD}/2$ DC level shift to the input. Although a 1:1 transformer is shown, a step-up transformer may be selected to reduce the drive requirements. A reduced signal swing from the input driver, such as an op amp, may also improve the overall distortion.

In general, the MAX1449 provides better SFDR and THD with fully differential input signals than single-ended drive, especially for very high input frequencies. In differential input mode, even-order harmonics are lower as both inputs (IN+, IN-) are balanced, and each of the inputs only requires half the signal swing compared to single-ended mode.

Single-Ended AC-Coupled Input Signal

Figure 9 shows an AC-coupled, single-ended application. The MAX4108 op amp provides high speed, high bandwidth, low-noise, and low-distortion to maintain the integrity of the input signal.

Grounding, Bypassing and Board Layout

The MAX1449 requires high-speed board layout design techniques. Locate all bypass capacitors as close to the device as possible, preferably on the same side as the ADC, using surface mount devices for minimum inductance. Bypass V_{DD} , REFP, REFN, and COM with two parallel 0.1 μ F ceramic capacitors and a 2.2 μ F bipolar capacitor to GND. Follow the same rules to bypass the digital supply (OV_{DD}) to OGND. Multi-layer boards with separated ground and power planes produce the highest level of signal integrity. Consider

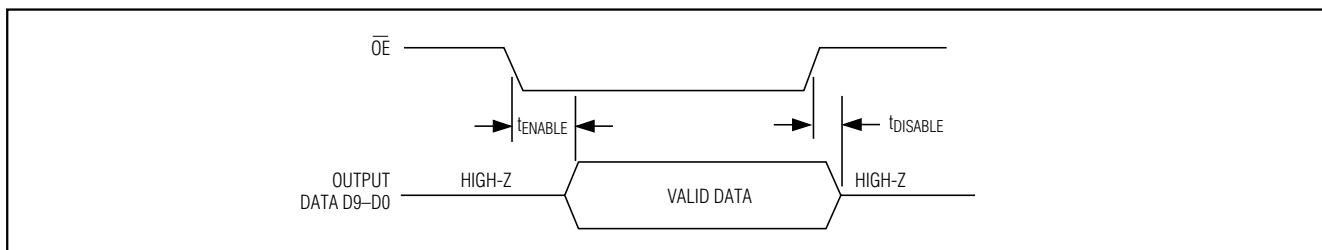


Figure 5. Output Enable Timing

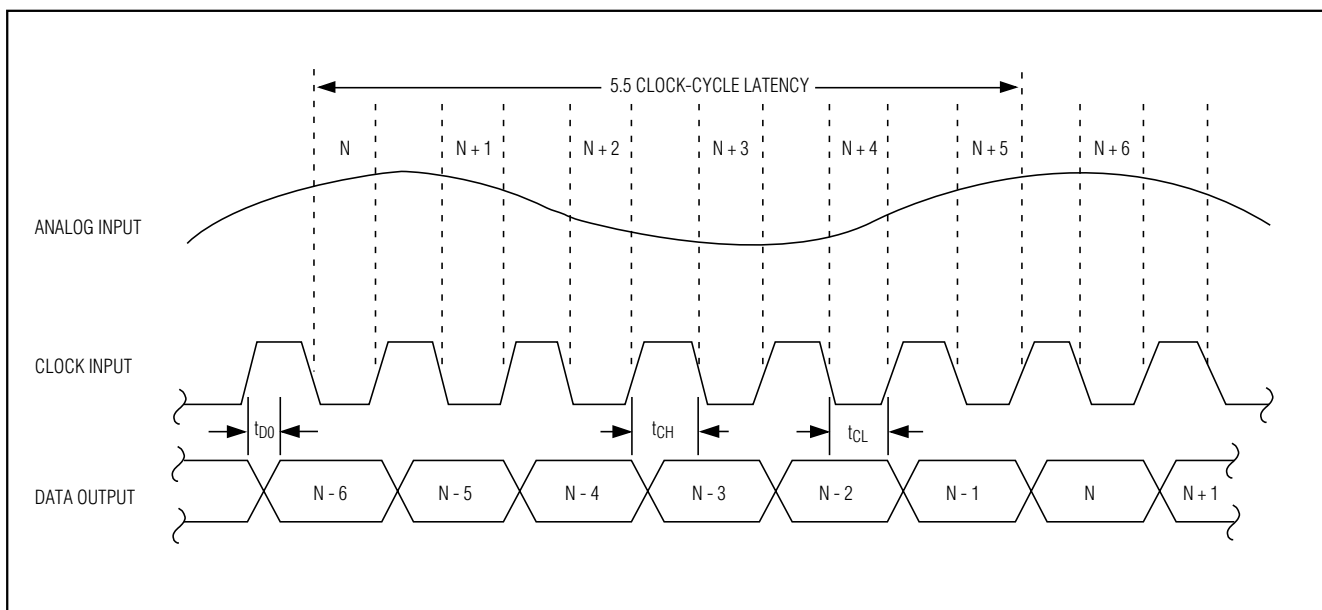


Figure 6. System and Output Timing Diagram

10-Bit, 105MSPS, Single +3.3V, Low-Power ADC with Internal Reference

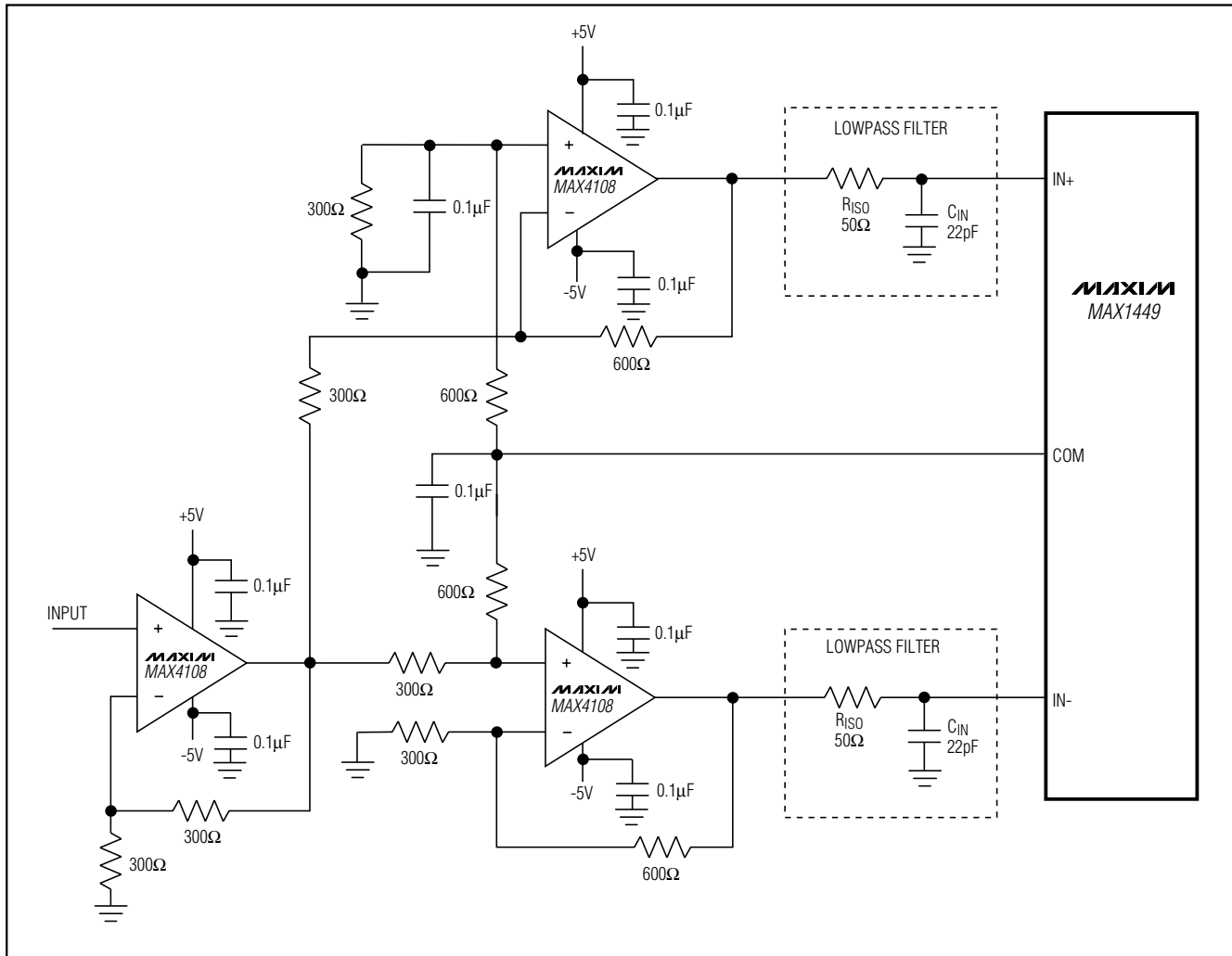


Figure 7. Typical Application Circuit Using the Internal Reference

the use of a split ground plane arranged to match the physical location of the analog ground (GND) and the digital output driver ground (OGND) on the ADC's package. The two ground planes should be joined at a single point, such that the noisy digital ground currents do not interfere with the analog ground plane. The ideal location of this connection can be determined experimentally at a point along the gap between the two ground planes, which produces optimum results. Make this connection with a low-value, surface-mount resistor (1Ω to 5Ω), a ferrite bead or a direct short. Alternatively, all ground pins could share the same ground plane, if the ground plane is sufficiently isolated from any noisy digital systems ground plane (e.g., downstream output buffer or DSP ground plane). Route high-speed digital

signal traces away from sensitive analog traces. Keep all signal lines short and free of 90° turns.

Static Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1449 are measured using the best straight-line fit method.

10-Bit, 105MSPS, Single +3.3V, Low-Power ADC with Internal Reference

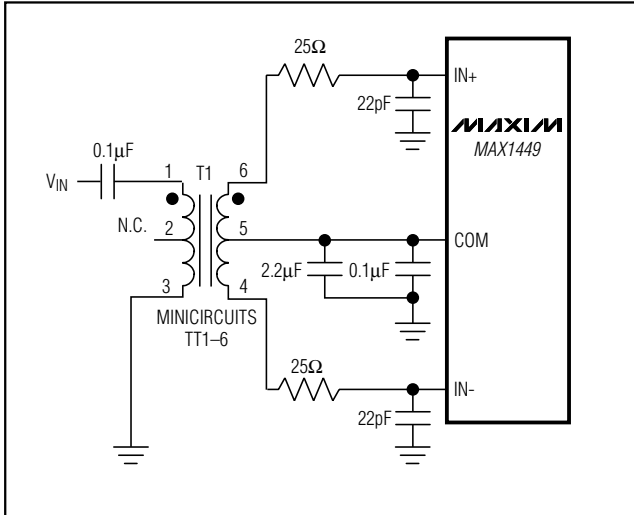


Figure 8. Using a Transformer for AC Coupling

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Dynamic Parameter Definitions

Aperture Jitter

Figure 10 depicts the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the falling-edge of the sampling clock and the instant when an actual sample is taken (Figure 10).

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N Bits):

$$SNR_{(MAX)} = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to all spectral components minus the fundamental and the DC offset.

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB is computed from:

$$ENOB = \frac{(SINAD - 1.76)}{6.02}$$

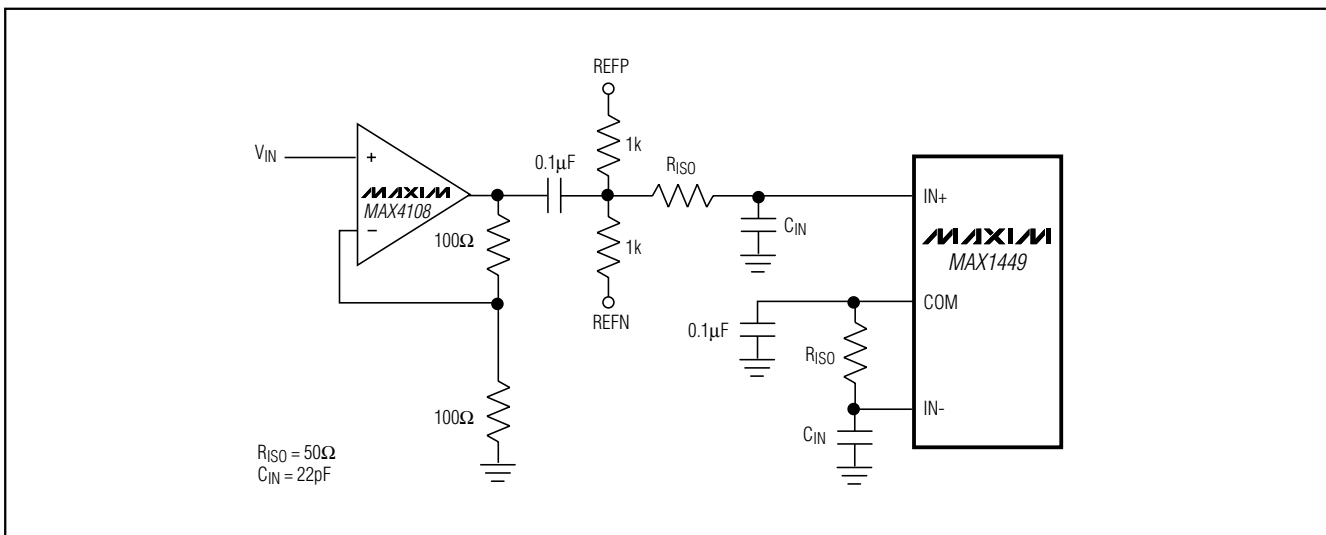


Figure 9. Single-Ended AC-Coupled Input

10-Bit, 105MSPS, Single +3.3V, Low-Power ADC with Internal Reference

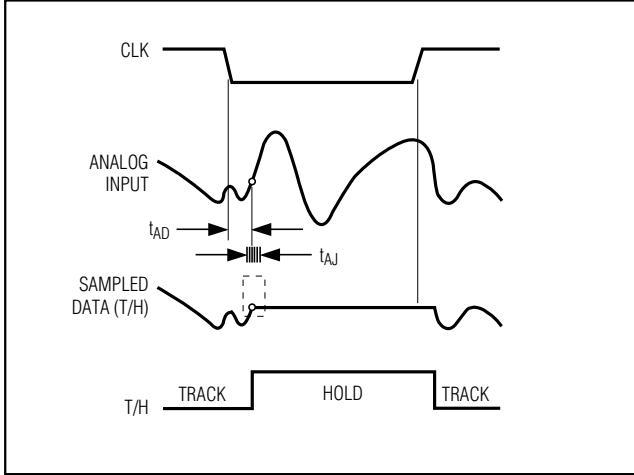


Figure 10. T/H Aperture Timing

Total Harmonic Distortion (THD)

THD is typically the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left(\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2)}}{V_1} \right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.

Intermodulation Distortion (IMD)

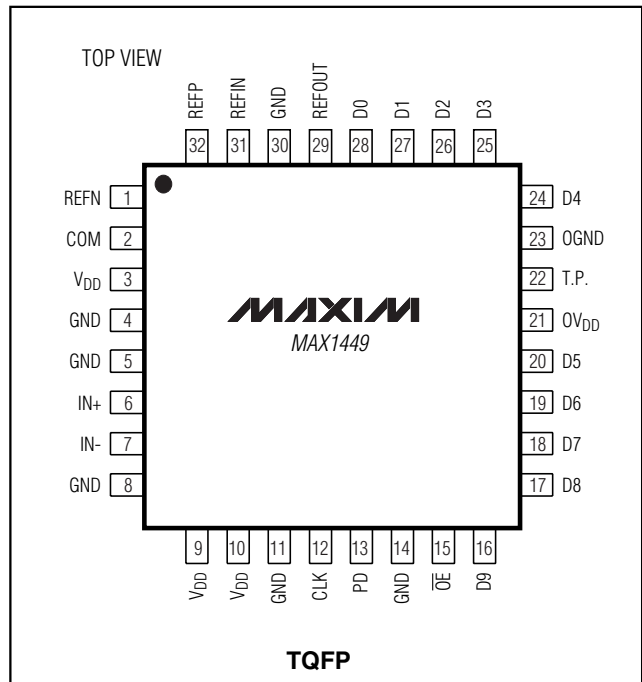
The two-tone IMD is the ratio expressed in decibels of either input tone to the worst 3rd-order (or higher) intermodulation products. The individual input tone levels are at -6.5dB full scale and their envelope is at -0.5dB full scale.

Chip Information

TRANSISTOR COUNT: 5684

PROCESS: CMOS

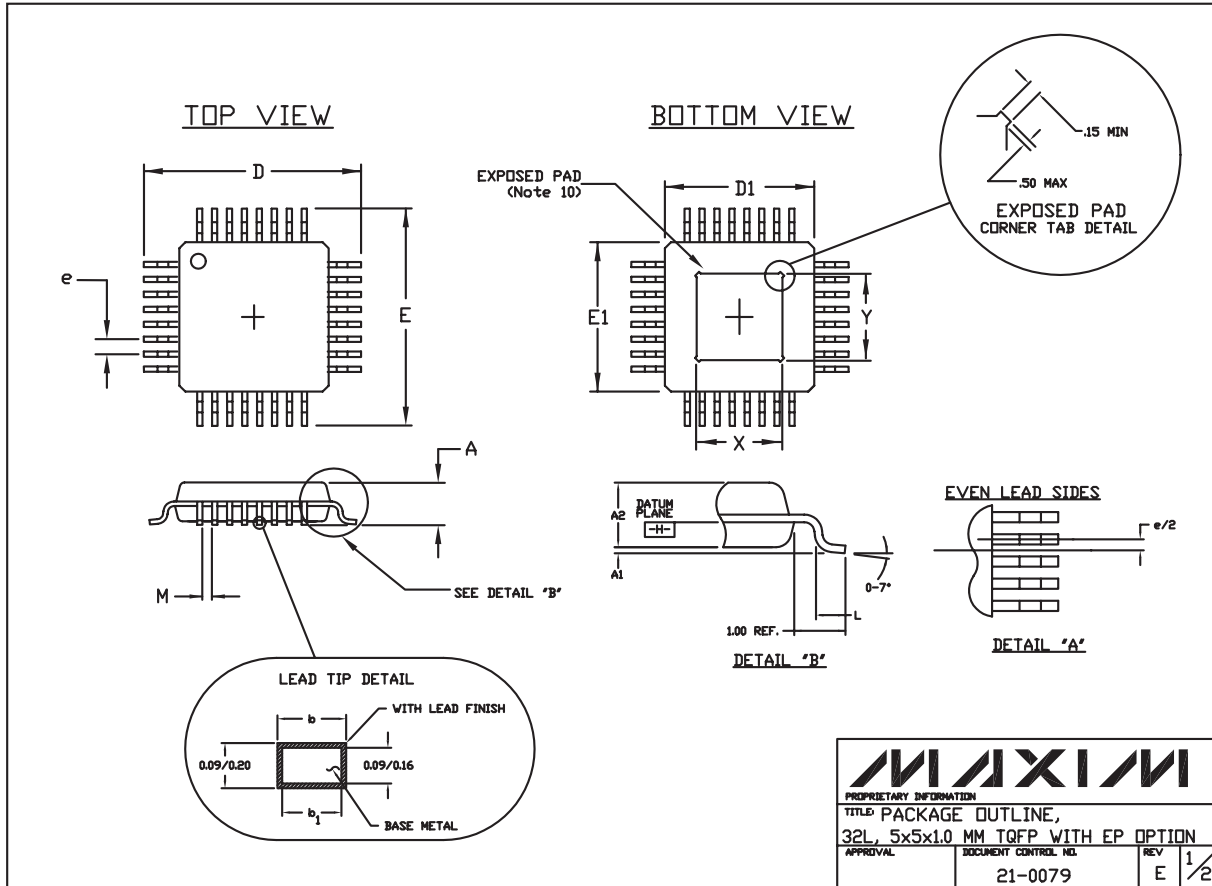
Pin Configuration



10-Bit, 105Mps, Single +3.3V, Low-Power ADC with Internal Reference

Package Information

MAX1449



10-Bit, 80MSPS, Single +3.3V, Low-Power ADC with Internal Reference

Package Information (continued)

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE \square IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MO-136.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.

JEDEC VARIATIONS				
DIMENSIONS IN MILLIMETERS				
AA		AA-EP*		
5x5x1.0 MM		5x5x1.0 MM		
	MIN.	MAX.	MIN.	MAX.
A	\approx	1.20	\approx	1.20
A1	0.05	0.15	0.05	0.15
A2	0.95	1.05	0.95	1.05
D	7.00 BSC.		7.00 BSC.	
D1	5.00 BSC.		5.00 BSC.	
E	7.00 BSC.		7.00 BSC.	
E1	5.00 BSC.		5.00 BSC.	
L	0.45	0.75	0.45	0.75
M	0.15	\approx	0.15	\approx
N	32		32	
e	0.50 BSC.		0.50 BSC.	
b	0.17	0.27	0.17	0.27
b1	0.17	0.23	0.17	0.23
*X	N/A	N/A	2.70	3.30
*Y	N/A	N/A	2.70	3.30

* EXPOSED PAD (Note 10)

<small>PROPRIETARY INFORMATION</small>			
TITLE: PACKAGE OUTLINE, 32L, 5x5x1.0 MM TQFP WITH EP OPTION			
<small>APPROVAL</small>	<small>DOCUMENT CONTROL NO.</small>	<small>REV</small>	<small>2/2</small>
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